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A CMOS slew-rate enhanced OTA for imaging

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ABSTRACT

CMOS Image Sensors have many applications currently. They are present everywhere and almost everyone owns many cameras based on these sensors ranging from mobile phones (with several cameras), to tablets, computers, security devices and cars. Although they work pretty well as we increase their resolution and quality we face a few problems. One of these problems is Flicker noise. The other source of noise, thermal, evolved a lot recently and flicker noise is now the main limitation regarding improving the performance. This work presents a new method to reduce the flicker noise contribution in the overall sensor noise by reducing the time for Double Sampling, allowing to filters more correctly the flicker noise spectrum introduced by the pixel source follower amplifier. We also introduce a way to remove the column induced lag that comes from the column readout circuitry by using strong and stable references. We propose a new amplifier that is used as a buffer for the reference voltage. At the same time Double Sampling is performed. This solution contributes both to reduce the current consumption and time between samples which also contributes to a lower power heat dissipation. The developed circuit can be seen as a generic solution for applications that need stable references and high resolution, resulting in a massively parallel circuit, as it is common in CMOS image sensors. The proposed solution is tested with a circuit containing 3000 readout columns.

1. Introduction

CMOS Image Sensors have many applications currently. They are present everywhere and almost everyone owns many cameras based on these sensors ranging from mobile phones (with several cameras), to tablets, computers, security devices and cars.

These sensors not only became very important to our daily life as we now frequently register data as images, as they evolved a lot in the last few years and although they work pretty well as we increase their resolution and quality we face a few problems. One of these problems is Flicker noise. The other source of noise, thermal, evolved a lot recently and flicker noise is now the main limitation regarding improving the performance.

In this work we presents a new method to reduce the flicker noise contribution in the overall sensor noise by reducing the time for Double Sampling, allowing to filters more correctly the flicker noise spectrum introduced by the pixel source follower amplifier. We also introduce a way to remove the column induced lag that comes from the column readout circuitry by using strong and stable references. We propose a new amplifier that is used as a buffer for the reference voltage. At the same time Double Sampling is performed.

This solution contributes both to reduce the current consumption and time between samples which also contributes to a lower power heat dissipation. The developed circuit can be seen as a generic solution for applications that need stable references and high resolution, resulting in a massively parallel circuit, as it is common in CMOS image sensors. The proposed solution is tested with a circuit containing 3000 readout columns.

This paper is an extended version of the conference paper "Design and simulation of a CMOS slew-rate enhanced OTA to drive heavy capacitive loads", from the same authors, presented at the workshop on Electronics Applications and System Integration for Future Technologies, being submitted to this special issue.

The rest of the paper is organized as follows: section II provides background and describes the problem being approached; section III is about High Slew-Rate Amplifiers and theirs state of the art; section IV presents the proposed solution; section V presents a preliminary simulation results and section VI presents the conclusions.

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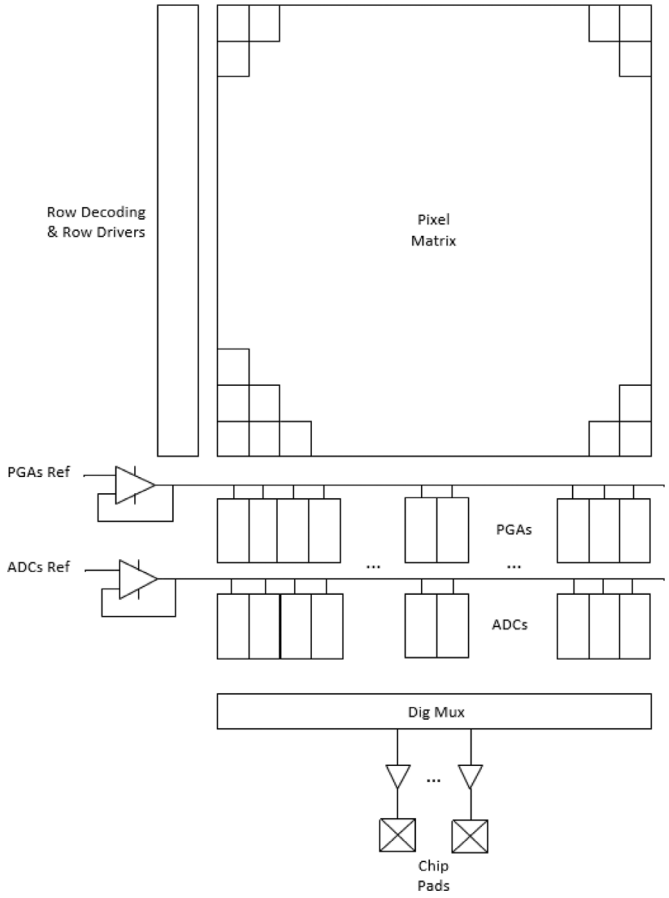

Fig. 1. Block diagram of a column parallel CMOS image sensor.

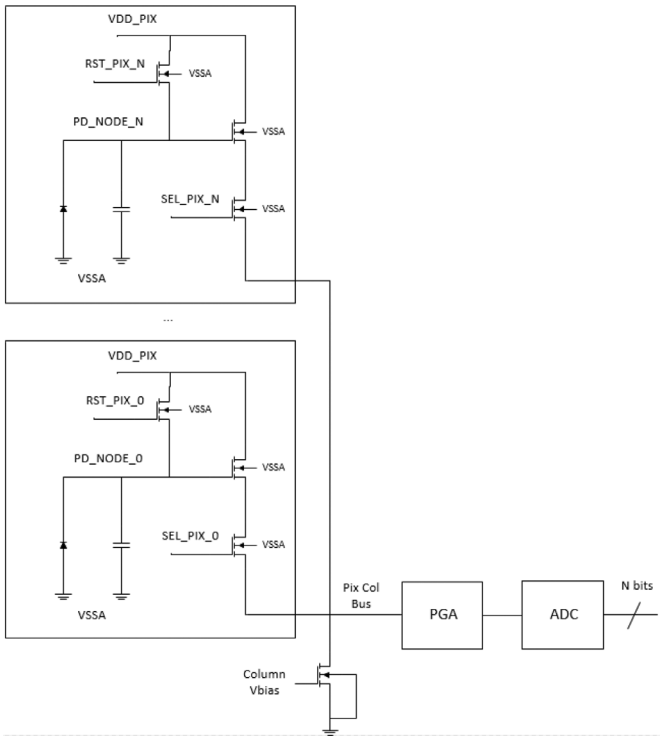

Fig. 2. 3T active pixel structure and column readout structure.

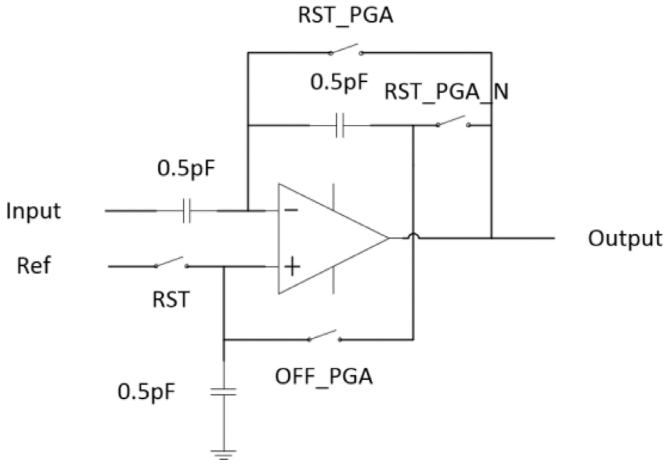

Fig. 3. Column PGA circuit.

2. Background

CMOS sensors are usually composed of a bi-dimensional pixel array, with the pixels containing an electrical potential proportional to the photon generated charges. For most current CMOS image sensor solutions, the structures have a standard composition, similar to the one shown in Fig. 1.

These structures make use of a Programmable Gain Amplifier (PGA) stage also because it helps reducing the contribution of noise from the initial stages but because it can perform a Double Sampling (DS) operation.

Pixel integration can be done with different circuits but probably the simplest circuit is the so called 3T active pixel, composed of a built-in pixel amplifier namely a Source Follower (SF) stage, which makes it an active pixel and with 3T indicating that the circuit is composed of 3 transistors. The SF device is biased by the column biasing current, set by the column NMOS device, by the time pixel is accessed when SEL_PIX signal goes from low to high level. Fig. 2 depicts a simplified version of the vertical array of pixels within a specific column.

This part works like this:

-By activating the SEL_PIX signal, a row of pixels is activated and the corresponding signal at the gate of pixel SF (PD_NODE) is read through the column and stored in the PGA stage. After the readout is terminated, the RST_PIX signal is raised to reset the pixel for the next pixel exposure/integration. The reset value is also sampled in the PGA stage so that the stage can build the difference between pixel signal and reset level. It is in the difference between these two voltage levels that there is the illumination information, or in other words, it is build the photo signal information.

A common design implementation of a PGA/DS stage is depicted in Fig. 3 (in this case with 0.5 pF capacitors and stage unitary gain). Its base circuit performs an integration operation, but it is a bit more complex. While the photo signal (at the pixel side) is obtained from the difference between the pixel reset and the signal voltage levels, at the PGA output, the photo signal is built-up from a known and stable reference voltage.

The timing diagram of the joint pixel photo signal and the double sampling (PGA) output signal, is depicted in Fig. 4. It shows different signal levels at the pixel column bus (with respect to different illumination levels), and their corresponding photo signals at the PGA output referred to the column amplification stage reference voltage.

For simplicity and clear understanding, we consider that the speed (to obtain two consecutive samples from the selected pixel), is not limited by the time to access the pixel, but rather dictated by how fast the PGA/DS stage performs its own offset cancellation.

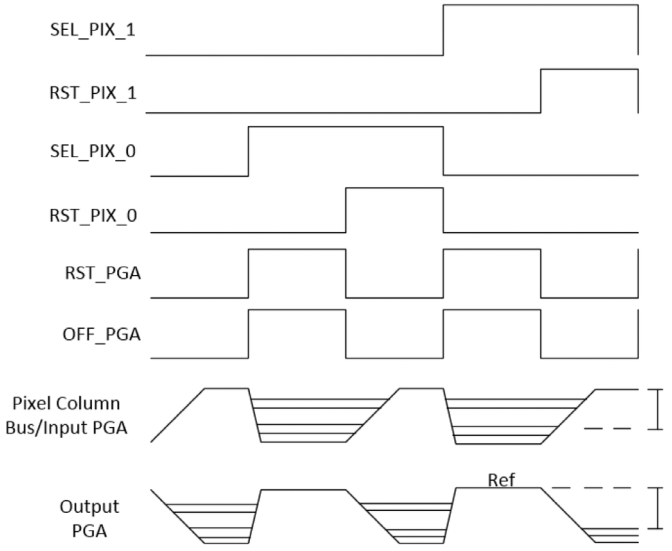

Fig. 4. PGA timing operation and pixel signals.

Image Lag is considered an artifact that usually happens related to the pixels and is due to incomplete pixel reset [1]. Somehow, it shows how much signal is left in the pixel PD_NODE (or sensing node) from the previous exposure (ideally none). This is a situation that happens due to abrupt light changes in consecutive integration cycles from high to low light intensity.

This more general idea can be also applied to the readout circuits, when a portion of the signal from the previous readout is present in the current conditioned signal, due to incomplete stage calibration (or offset cancellation). Given this, and based on the expected PGA circuit operation, if the offset cancellation process is effectively performed (by means of maintaining a stable reference and operating as Fig. 4 shows), we can ensure that no image lag induced by the column circuitry will occur, totally removing the photo signal from previous integration from the feed-back capacitor on the PGA.

The sampling and correlated subtraction is performed while the PGA offset cancellation is taking place. Additionally, the Flicker noise (sometimes called as 1/f noise and is present in both samples) can only be effectively reduced, as long as the stage calibration is effectively done and zeroed. Moreover, for simplicity we will consider large Full-Well Saturation 3T pixels such that pixels exhibit low KT/C reset noise power, compared with flicker noise power introduced by pixel SF.

The offset cancellation requires some time, and this time dictates the efficiency of the flicker noise reduction. The goal of this work is also to cancel the offset as fast as possible (with strong light/photo signal – which is the worst case), meaning that to some extent, the driver for the PGA's reference needs to be very strong, given that it has to supply thousands of PGA/DS stages, in accordance to Fig. 1.

The 1/f noise is a random, with zero mean and a low frequency noise signal, whose values at distinct times are highly correlated. Fig. 5 shows the principle of flicker noise reduction with the analogue DS operation and how its effect is mitigated by a shorter sampling period, Tds, which is limited by the shortest time that allows for stage calibration.

The DS transfer function (from the output flicker noise power perspective) is as follows [2]

$$Yn(j\omega) = Xn(j\omega) \times H(j\omega) = X(j\omega) \times \left[1 - e^{-j\omega\tau}\right] \quad (1)$$

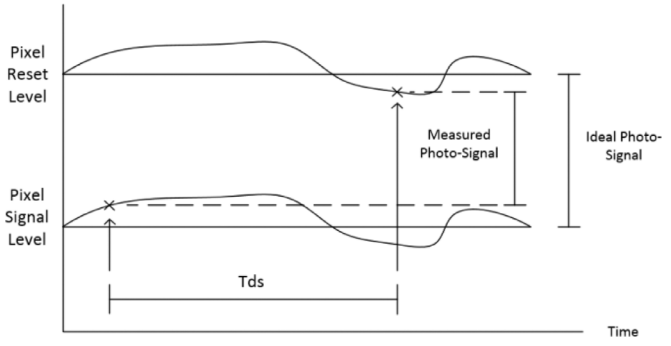

Fig. 5. Example of the time domain flicker noise correlation.

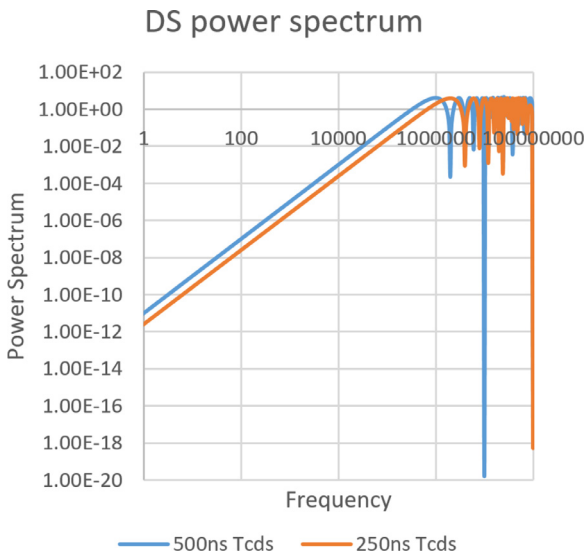

Fig. 6. System DS transfer function power spectrum.

Where τ refers to the time between samples. The amplitude power spectrum is also given by [2]

$$\left|1 - e^{-j\omega\tau}\right|^2 = \left|2e^{-j\left(\omega\frac{\tau}{2} - \frac{\pi}{2}\right)}.\sin\left(\omega\frac{\tau}{2}\right)\right|^2 = 4\sin^2\left(\omega\frac{\tau}{2}\right) \quad (2)$$

This function will shape the flicker noise power spectrum over the frequency, such that the total noise power integrated over the frequency is reduced (in case of a shorter sampling period). In Fig. 6 there is an example of two different transfer function amplitude power spectrums for different DS sampling periods, for 500 ns and 250 ns respectively.

The orange Power Spectral Density (PSD) wave, results from a shorter sampling period, while the blue PSD wave is for higher DS time. We can observe that with a shorter time between samples, the system operation will restrain more the 1/f noise power spectrum when compared with a longer sampling period.

It is therefore essential to reduce the DS period (or PGA offset cancellation time) in order to have less flicker noise contribution at the output, given that noise in both samples are highly correlated. Additionally, it is important to make sure that no image lag induced by column circuitry will occur, which in turn has implications to ensure proper stage calibration/offset cancelation by having a stable reference.

3. State of the art for high slew-rate amplifiers

To address the requirement of a strong reference driver circuit, the state of the art for high slew-rate amplifiers was analyzed to try to find an available solution for this feature.

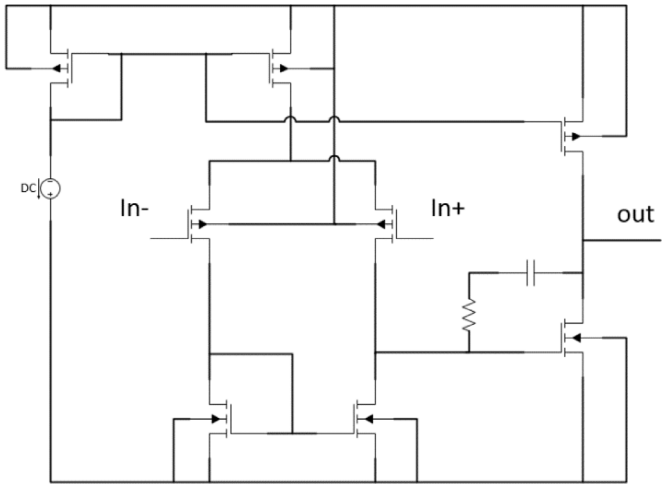

Fig. 7. Two-stage CMOS Miller amplifier with RHP zero cancellation resistor.

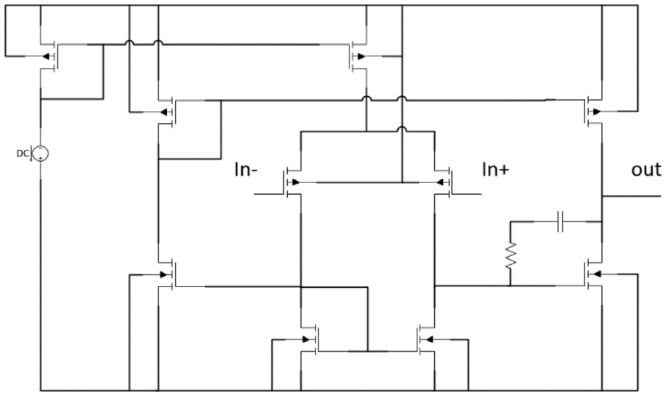

Fig. 8. Two-stage CMOS Miller amplifier with replicating branch.

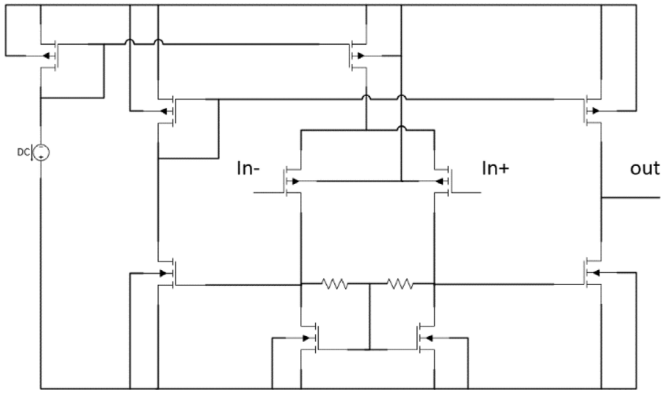

Fig. 9. Two-stage balanced LCMFB high SR amplifier.

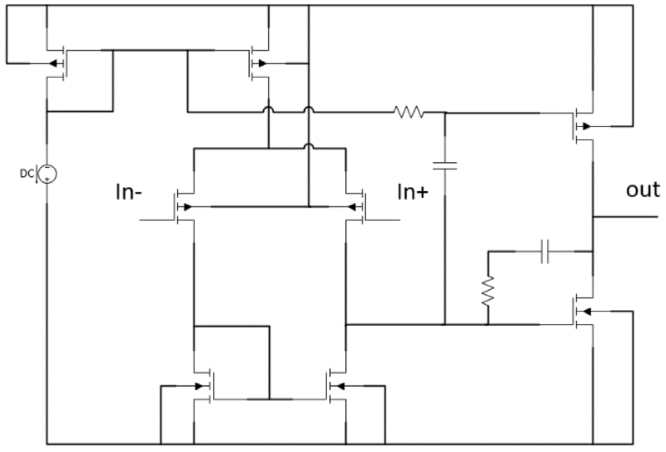

Fig. 10. Two-stage CMOS Miller amplifier with balanced AC coupled enhanced SR.

Most of the high Slew-Rate (SR) amplifier architectures are able to drive large capacitances (in a short period of time), unless large DC nominal current consumption is considered for them, which is often prohibitive in image sensors as they are required to work in low power, or they can drive large capacitive loads but suffering from some sort of undesired limitation. This work highlights some of these.

The first amplifier to be considered was the well-known Two-stage CMOS Miller amplifier [3], depicted in Fig. 7. It is known to exhibit uneven slew-rates, either by supplying or sinking output current, depending on the input pair device type. It exhibits high slew-rate for one side, in contrast to being slew rate limited (with a fixed current) on the other side.

The second amplifier to be considered is the replicating branch Two-stage CMOS Miller amplifier [4,5] that improves the fixed output current from one side branch (by the amount of the current mirroring factor) with respect to the high SR from the other side, depicted in Fig. 8.

It can seem from the literature that this circuit does in fact improve the SR limitation although it does not achieve full output balanced currents.

Another amplifier which has been considered, uses an input differential pair stage with differential outputs, performing a Local Common Mode Feedback (LCMFB) [6], promoting a high SR for both source and sink output currents (shown in Fig. 9). The version shown, for simplicity sake, does not include the cascaded devices.

Observing Fig. 9, one can notice that to have stable inner stage output Common Mode (CM) voltage, it uses an internal CM correction loop composed of resistors, which in turn limits the output resistance of the inner stage, therefore limiting the overall amplifier gain. As a consequence, it reduces a bit the ability of achieving high open-loop gain, although it's capable to generate a balanced high output current, while exhibiting high output SR.

Another solution based on the AC coupling effect [4,5,7] to achieve enhanced output SR can be seen in Fig. 10.

For this solution, between the output up and down MOS transistors, a voltage is created in steady state such that during a transient event, (considered to require a large amount of output current), the down side gate signal is capacitive coupled to the up side gate device creating an AC coupled effect, enhancing the output SR. In the same way as for the previous circuit from Fig. 9, the amplifier from Fig. 10 is capable of providing a balanced output current, however both amplifiers are somewhat limited in their output SR. The limitations are due to the gates of the output devices that have limited swing, dictated by the inner stage output swing, which in turn depends on the amplifier input common mode voltage.

Another type of effective SR enhancement amplifier is depicted in Fig. 11, showing a different concept for high output SR Operational Trans-conductance Amplifier (OTA), called Automatic SR enhancement OTA with auxiliary circuit. The circuit is composed of a P-type input push-pull amplifier assisted by an auxiliary (amplifier) circuit. In fact it exhibits a functioning behavior that will be later shown to be somehow similar to the one proposed in this paper, because it draws current in the discrete-time domain. To do so, it is necessary to create a sufficient input difference to trigger an

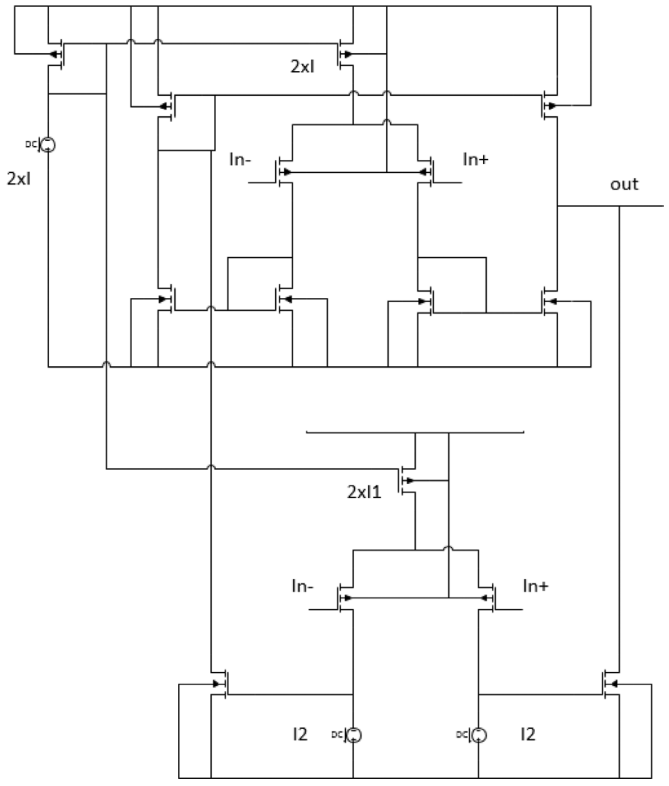

Fig. 11. Automatic SR enhancement OTA with auxiliary circuit.

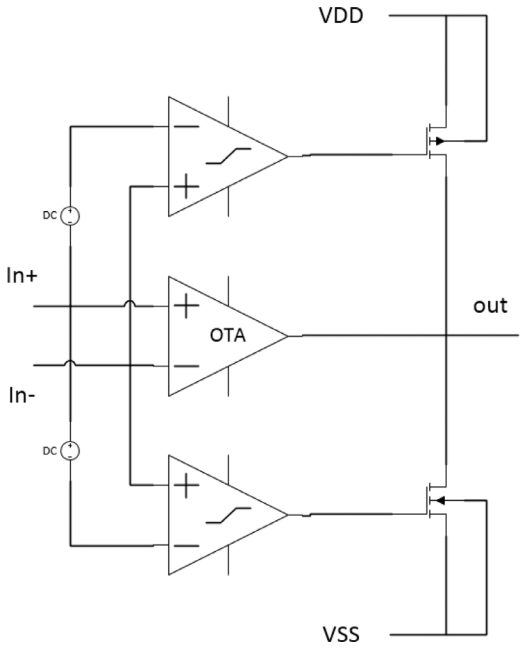

Fig. 12. Proposed amplifier structure with automatic and balanced SR enhancement OTA.

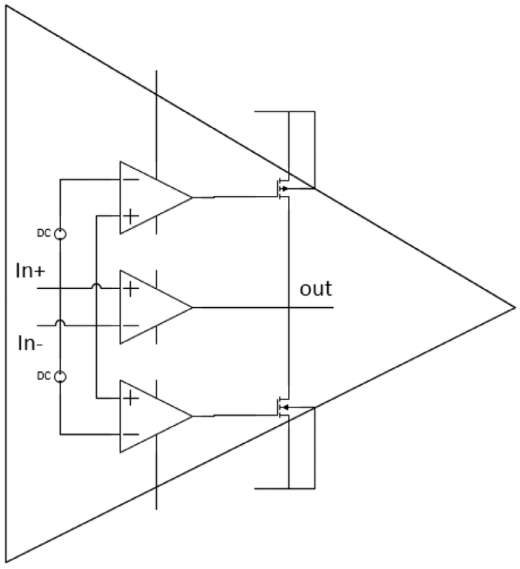

Fig. 13. Equivalent block level symbol of the proposed amplifier structure.

auxiliary circuit [8]. For proper operation, I2 current must be bigger than I1 current. The trigger point is defined by designer during the amplifier construction, by means of defining the I2/I1 ratio.

After analyzing the state of the art and presenting the most relevant solutions we consider that none of the presented solutions solves our requirements not generating balanced output current or not providing enough SR. Therefore we propose achieving high output and balanced SR in a different way, as it will be reported in the following sections.

4. Proposed solution

As pointed out before, our proposed solution consists of SR enhanced amplifier that contains an auxiliary circuit, in discrete-time domain, that is automatically activated during transient events, if solicited. A schematic view can be seen in Fig. 12.

The circuit works in the following way: when negative input (IN-) voltage drifts from positive input (IN+) by a predefined amount (during a transient event for both open or closed loop configuration), the whole stage will source or sink large output currents to satisfy the need of the amplifier to bring inputs close to each other, by activating an auxiliary circuit. The trigger point to activate the auxiliary circuit is defined by two DC threshold voltages fixed to the IN+ input. When the SR enhancement circuit, composed of the top and bottom OTAs, is activated, it creates a pulse width signal modulated with the time that IN- input is out of the range created by these thresholds.

The goal of this architecture is such that it can be applicable to a variety of amplifier structures, without increasing quiescent current from the main amplifier. Meaning that, if the output node is inside the range of the threshold voltages, the main amplifier is the only circuit that drives the load. However, if the output goes outside the thresholds, it triggers the SR enhancement auxiliary circuit and draws a pulsed current for as long as it is needed to bring the output node inside the defined threshold range. After this, the main amplifier (the middle one), drives the load alone again. This creates a non-DC current consumption that needs to be handled with proper on-chip power routing and decoupling, in order not be seen as an environmental noise source to other sensitive circuits.

Additionally, the gate of the output devices swings from rail-to-rail supplies, taking the maximum advantage of them to enhance the output slew-rate, for a given size of the output auxiliary devices. Another feature of this block level implementation amplifier architecture, is that it can be used and seen like a regular 3-pin amplifier, with two differential inputs and one single ended output, as represented in Fig. 13.

The proposed circuit can also be used independently of the type of the main OTA and in all situations a high output and balanced SR are required, especially in those situations that need an automatic activation of the extra pulsed current, despite the main am-

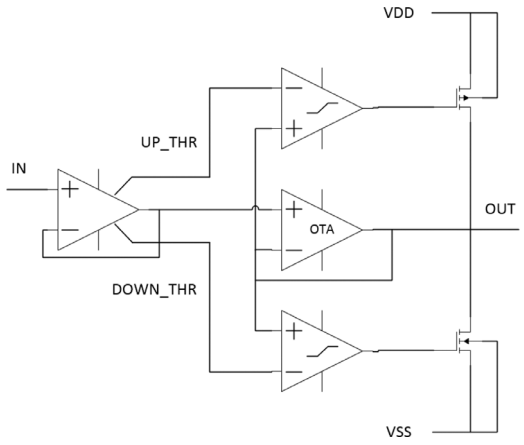

Fig. 14. Practical design implementation of the proposed high SR amplifier.

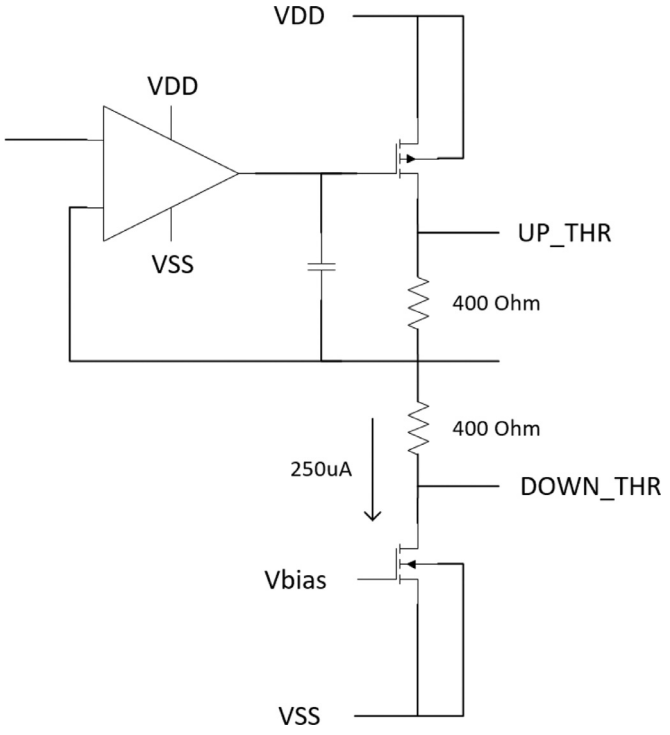

Fig. 15. Practical design implementation of the theshold voltages generation.

plifier topology, and feedback configuration, which allows it to be seen as regular amplifier.

5. Simulation of the proposed solution

This section consists of two sub-sections, one with a preliminary simulation to establish the comparison terms with other solutions and another one considering real working condition.

5.1. Preliminary simulation

A preliminary simulation was prepared using a unitary gain configuration and 1 nF load, as this is the expected load inside the image sensor.

To compare with the literature, the balanced LCMFB amplifier (from Fig. 9) was tested as well in the same test bench.

In Fig. 14, we can see the practical design implementation of the proposed solution, while Fig. 16 shows the adopted simulation setup.

Compared to what was shown before, one can notice the presence of an additional input amplifier stage. This is done to obtain the internal threshold references, with an additional input amplifier that produces 250uA, flows into 2 series resistors of 400Ohms each, performing a total threshold range of 200 mV (+100 mV and −100 mV). The threshold voltages generation scheme can be seen in Fig. 15 in greater detail.

The circuitry (to form threshold voltages) is connected such that its system output node connects to the positive input node of the amplifier. This is needed to ensure a negative feedback topology given that the output branch circuitry adds 180° signal phase. With such scheme, it is possible to generate an output voltage that follows the input, with 2 extra output nodes, +/−100 mV away from the output one.

The voltage generation process is illustrated in Fig. 17, where the high SR triggering pulses are highlighted, when a severe output voltage change happens requesting large output current from the amplifier structure. The wave's information clearly highlights that whenever the system output node is outside the references range, the auxiliary circuit triggers the Up (sourcing current) or Down (sinking current) pulses in order to bring the output inside the threshold range. Once output node is in that range, the middle amplifier takes control over the system dynamics, being its responsibility to settle the output node with a finer error.

Fig. 18 shows all the output voltages ("Out_Boost" - green, "Out" - blue and "Out_Diff_Balanced" – yellow, output nodes) and their derivatives, while Fig. 19 shows all the currents flowing from VDDA and to VSSA ports from each amplifier type. From this image one can easily see that there is a clear advantage with respect to the output current capabilities for both high SR amplifiers, compared with the regular rail-to-rail push-pull OTA, as is expected.

The reader may note that, from Fig. 18 onwards, wave's color corresponds to the same block on all upfront figures, so that comparison becomes easier.

The LCMFB amplifier was designed such that its quiescent current is equal to the proposed amplifier structure, consuming both 6.2 mA, to provide a fair comparison. On the other hand, the nominal DC current consumption for the regular rail-to-rail input OTA is roughly 5.2 mA.

Figs. 18 and 19 demonstrate the ability of the proposed amplifier circuit output node to settle faster (green wave) compared with regular rail-to-rail push-pull OTA output node (blue wave) for a 1 V step input signal (500 ns width pulse). Also, the increasing factor of output SR performance is much higher compared with the slightly increase of the nominal current.

From Fig. 19, we can also notice that the proposed amplifier structure has an even supply current distribution for both input signal transitions (green waves), while for the LCMFB amplifier, it generates an uneven supply current profile (yellow waves) as the VSSA port has to absorb more current compared with the current that VDDA port has to supply. This can lead to an additional issues to deal with, if on-chip power decoupling is not made adequately.

Fig. 20 shows a close up view of the proposed boosted and the LCMFB amplifier output nodes. The boosted output node (green voltage wave), exhibits higher slew rate compared with its competitor LCMFB (yellow voltage wave), although the first one shows a higher delay, evidencing a shorter bandwidth. On top of that, the preliminary simulation has shown that the rail-to-rail push-pull OTA can deliver a limited output current of 4 mA and the proposed structure amplifier can deliver roughly an average current up to 17.3 mA, while the competitor LCMFB amplifier is able to deliver roughly an average current up to 12.9 mA.

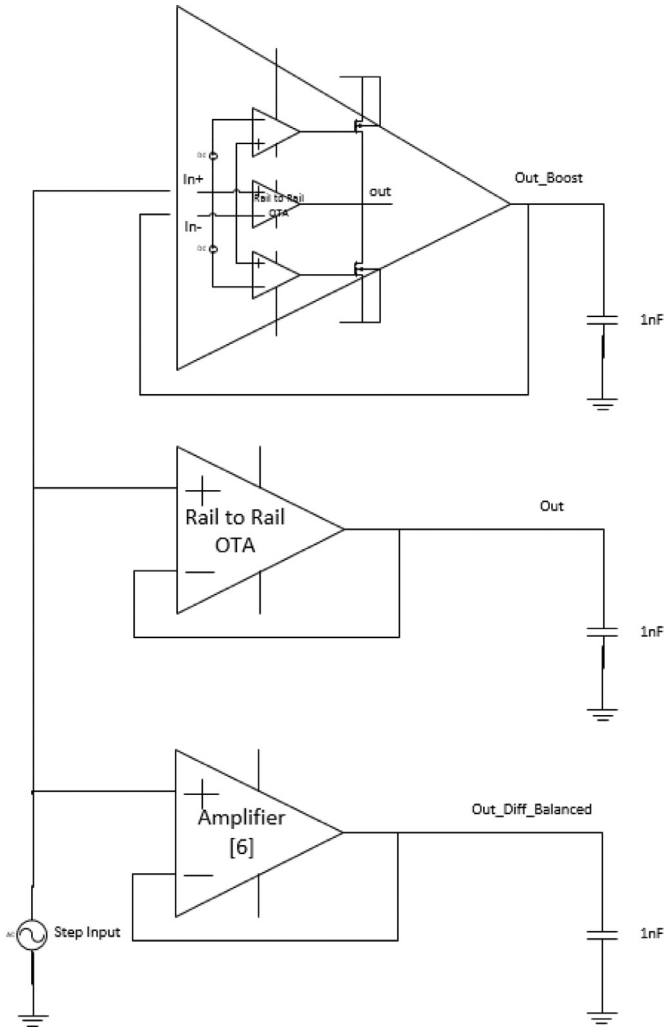

Fig. 16. Simplified view of the preliminary test bench, comparing the proposed amplifier with regular rail-to-rail input OTA and with the LCMFB amplifier [6].

To tackle the delay issue, which adds settling time to the system response, an AC analysis was performed to check the frequency domain behavior of both relevant circuits. Fig. 21 depicts the simulated open-loop gain of each relevant amplifier, as a function of the frequency. They exhibit distinct open-loop gain and bandwidth. Given that the amplifiers are supposed to be connected in a unity gain closed-loop configuration, the 0 dB frequency is the one of interest. As a matter of fact, the observed delay in the step response for the proposed circuit compared with its competitor, comes from the smaller 0 dB frequency (visible on the Bode Plot).

Despite the small delay issue, the main rail-to-rail OTA (proposed in this work) exhibits higher open-loop gain when compared to the LCMFB counterpart, meaning that it can be used in precision applications as a reference driver

In this case, the interest is to explore the enhanced SR capability to perform offset cancellation of the 3000 PGA stages faster, while using DS in the analogue domain. The goal is to be able to contribute in reducing the flicker noise (by shorting the time between pixel reset level and integrating signal samples) and by at the same time, to ensure that no light signal dependent artifacts (by effective offset cancellation), i.e. image lag is induced by the column circuitry.

The proposed amplifier structure quiescent current and output SR performance are summarized in three tables. Table 1 reports the raw performance metrics, while Tables 2 and 3 compare amplifiers in equivalent conditions: slew-rate and quiescent currents.

Preliminary results for the test case driver, can be rearranged in order to quantify the resulting improvement in output SR, for the proposed amplifier structure. To do such comparison, we have considered the same quiescent current, and considered also that the output current pulses are scaled down in same proportion as the quiescent current is.

On the other hand, we can retrieve additional information about equivalent DC current consumption for equal output SR conditions.

From these results, it is possible to conclude that there is a considerable output SR improvement factor, higher than 3.6x when compared with the regular rail-to-rail push-pull OTA, and a 1.34x higher SR than its competitor LCMFB, exhibiting 34% more output SR, for equal conditions of amplifiers quiescent current. On the other hand, we can say that for equal output SR capabilities, we

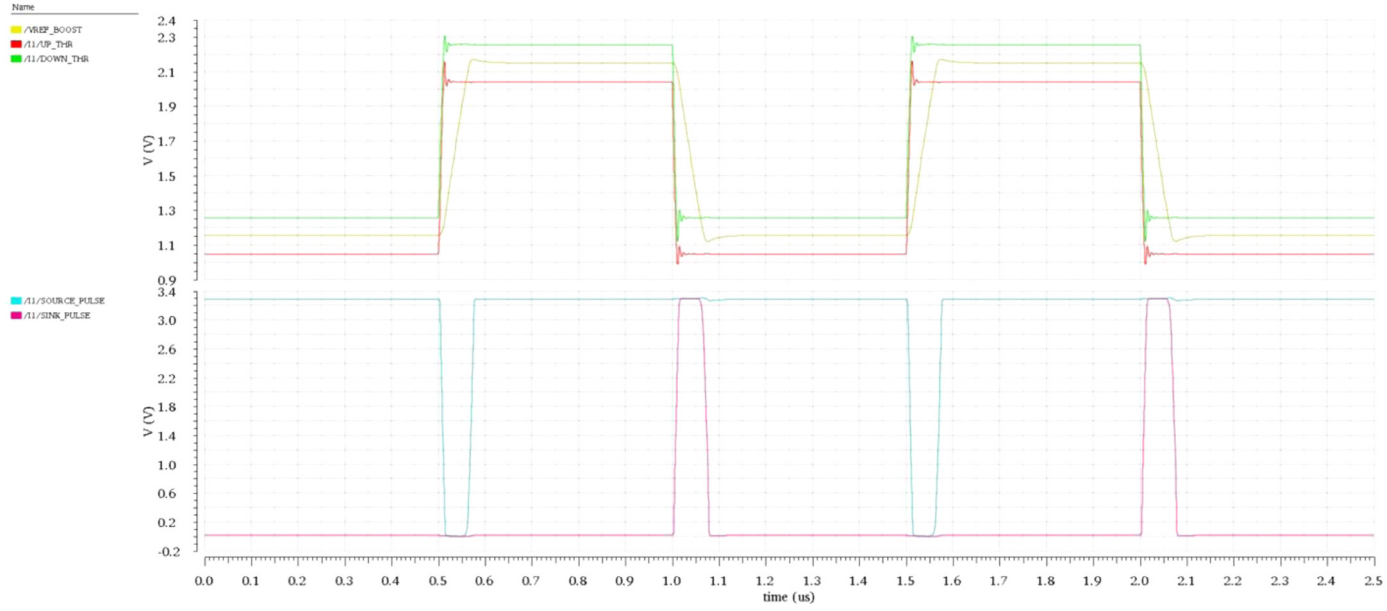

Fig. 17. Proposed amplifier structure threshold voltages generation and trigering of the high SR pulses, at 1 V output voltage step with a 1 nF load.

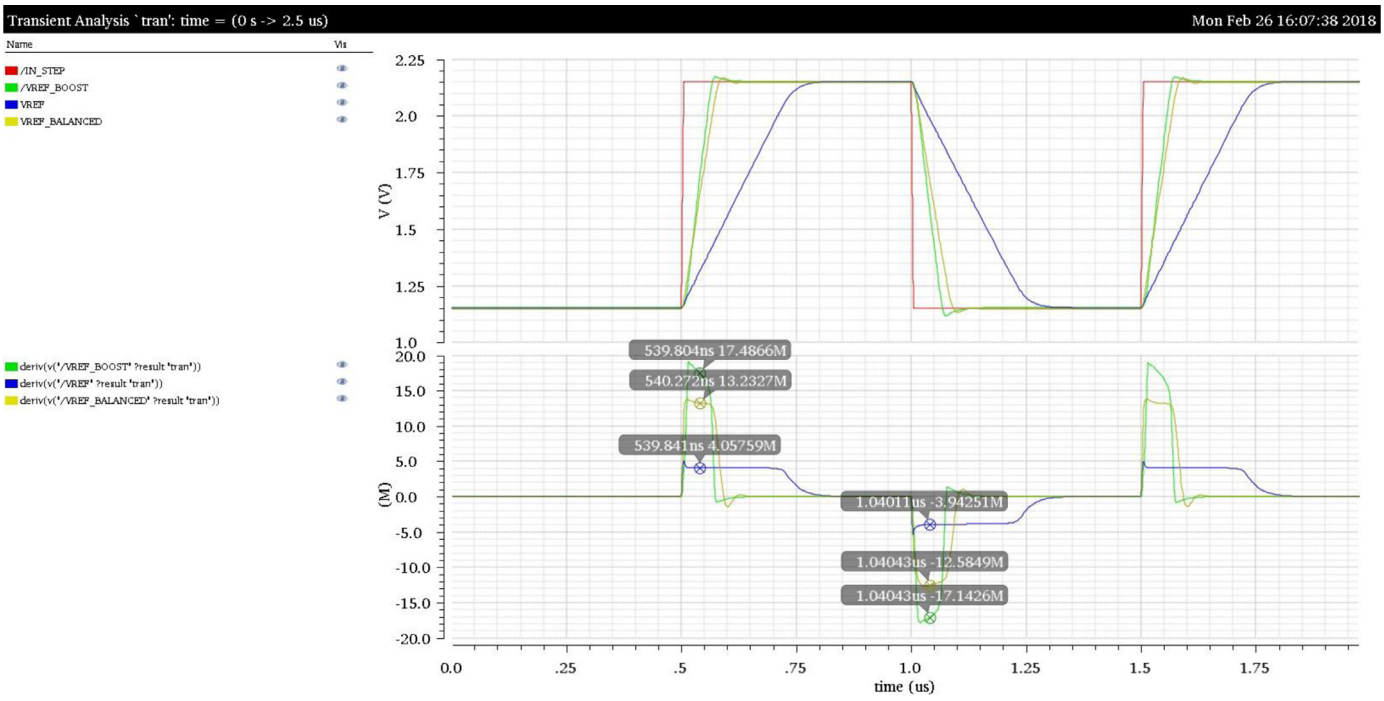

Fig. 18. Step input and corresponding output wave forms from the preliminary simulation test bench.

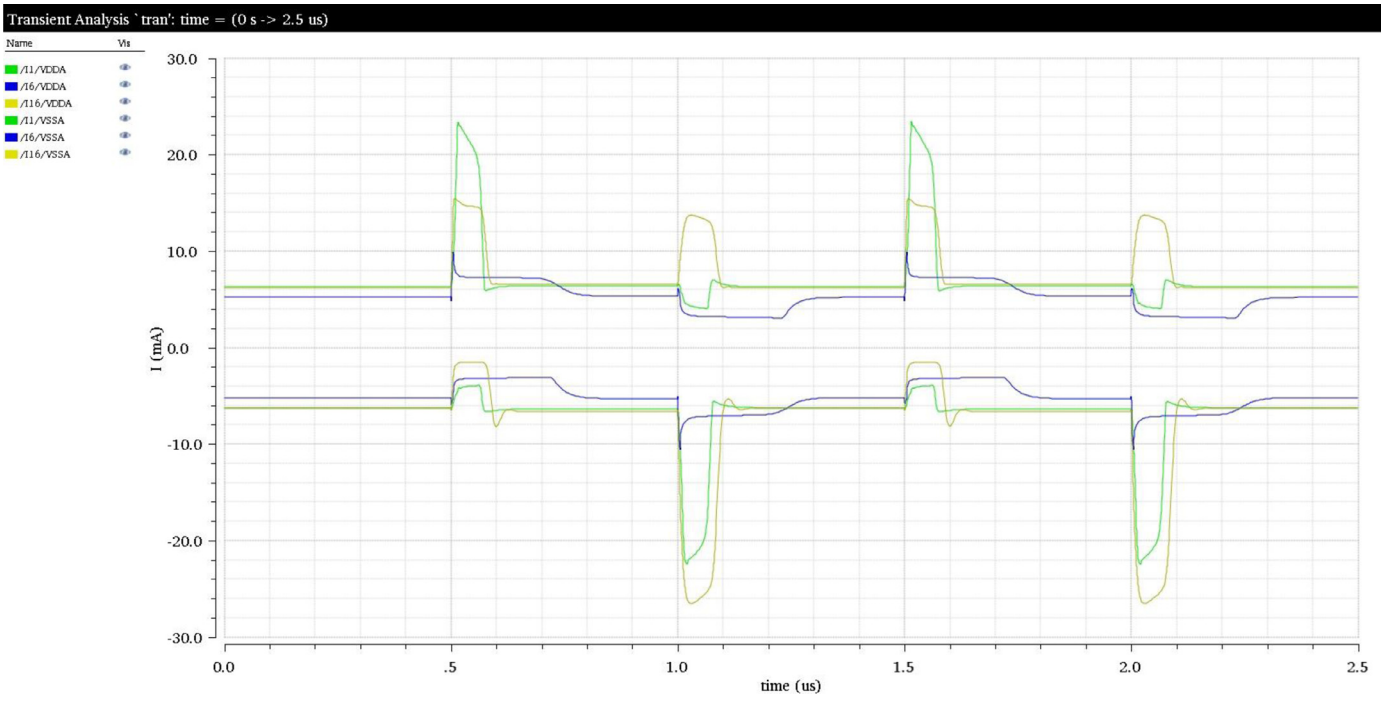

Fig. 19. Total blocks IO supply port currents.

can reduce power consumption (by using the proposed architecture) by a factor of 3.6x and 1.34x compared with the single rail-to-rail amplifier and its main competitor, respectively.

5.2. 3k cap load simulation results

The previous section showed us promising results for a pure capacitive load. Nevertheless, the real case is when the driver circuit not only has to deal with the overall tied capacitance but also with the dynamics of thousands of column amplifier stages. To be sure that our proposed circuit is able to respond correctly here, a more realistic simulation was setup with 3000 PGA stages, as depicted in Fig. 22. To simplify the diagram, the driver has been draw as a regular amplifier, but with the indication that it has high SR capabilities.

Fig. 23 shows the simulated reference voltages settling time for the proposed architecture, rail-to-rail main OTA and the LCMFB amplifier, each driving 3000 PGA stages.

The simulated system operation depicted in Fig. 23, is in line with the timing on Fig. 4. While the PGA is kept in reset phase (by activating RST signal of PGA), the integrated pixel signal is readout from the column bus, in accordance with Fig. 2 scheme. After the PGA offset cancellation occurs, the photo signal can be constructed

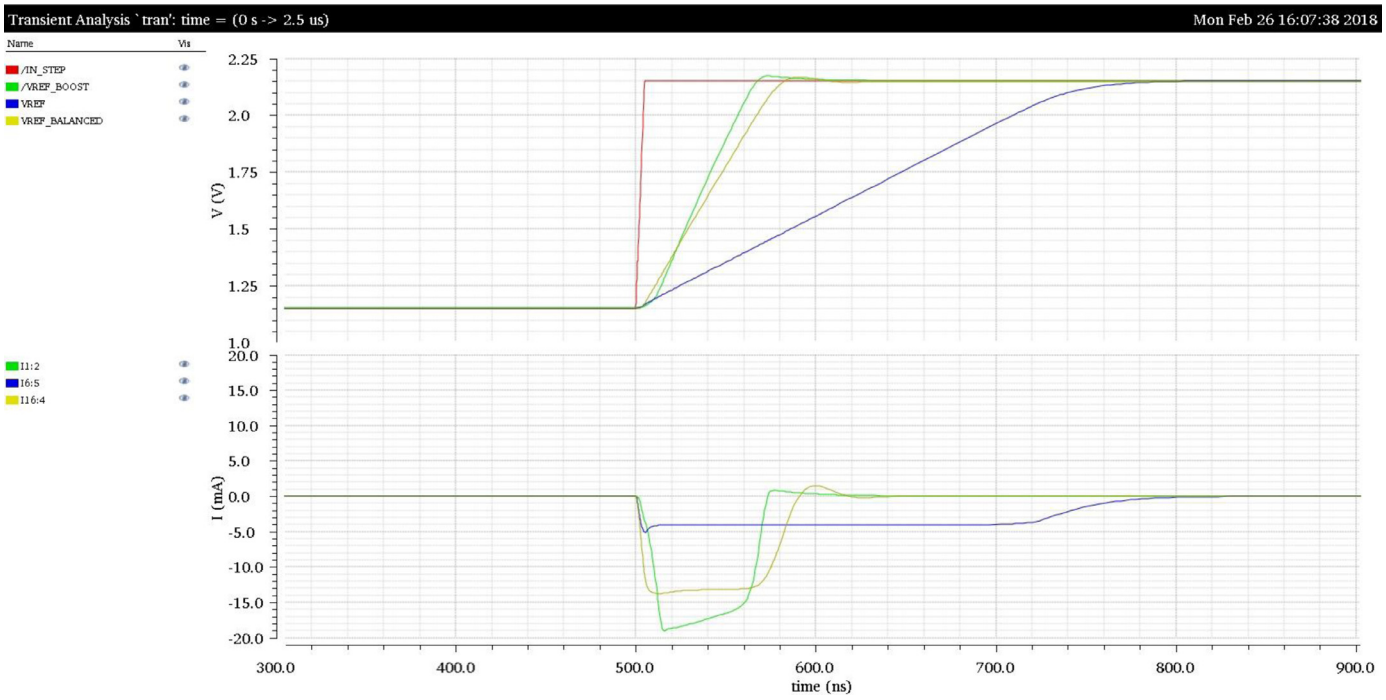

Fig. 20. Close up view of both proposed boosted and LCMFB amplifier nodes and their delay response to the step input.

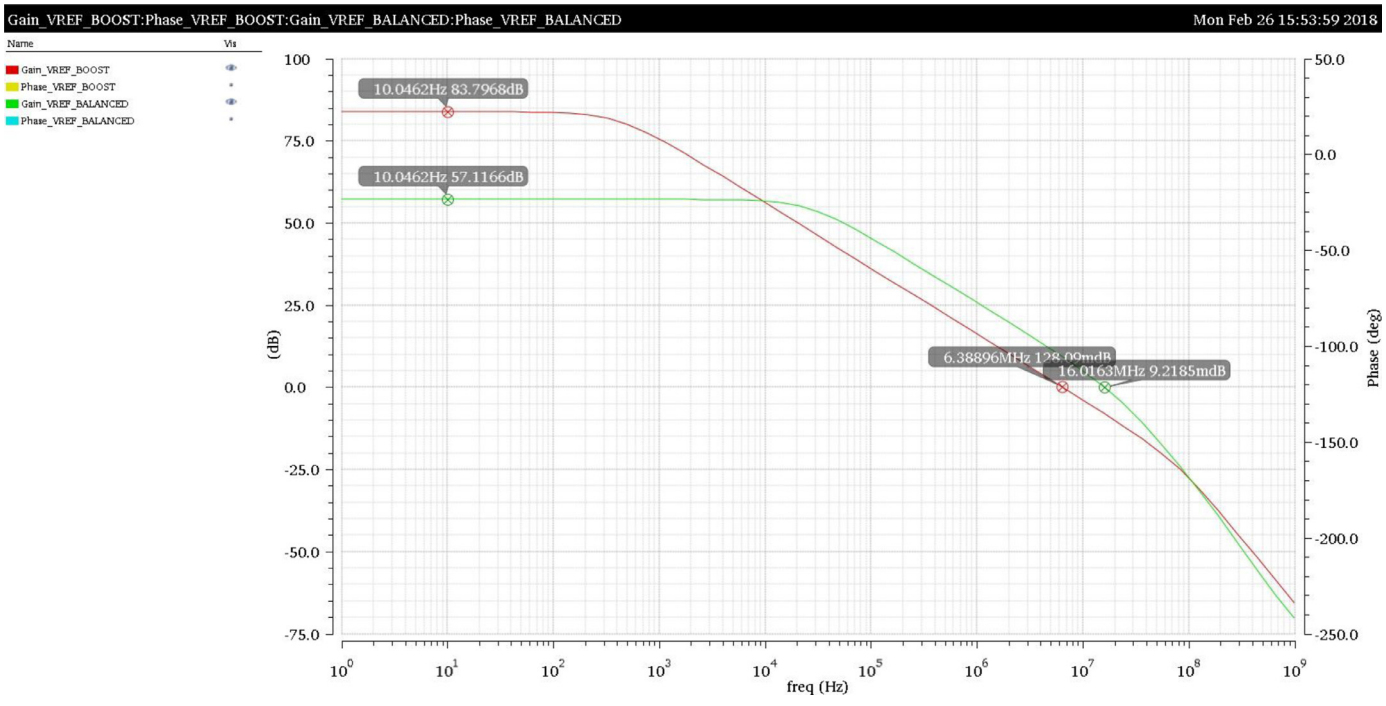

Fig. 21. Proposed boosted and LCMFB amplifiers AC open-loop gain.

Table 1
Summary of the preliminary simulation results.

	Quiescent current (mA)	Output current (mA)	Output slew-rate @ 1 V @1 nF (V/us)
Proposed amplifier structure	6.2	17.3	17.3
Single main amplifier	5.2	4	4
Competitor diff. balanced amplifier	6.2	12.9	12.9

Table 2
SR comparison at equal current consumption.

	For equal DC current consumption of 5.2mA Output slew-rate @ 1 V @1 nF (V/us)
Proposed amplifier structure	14.5
Single main amplifier	4
Competitor diff. balanced amplifier	10.8

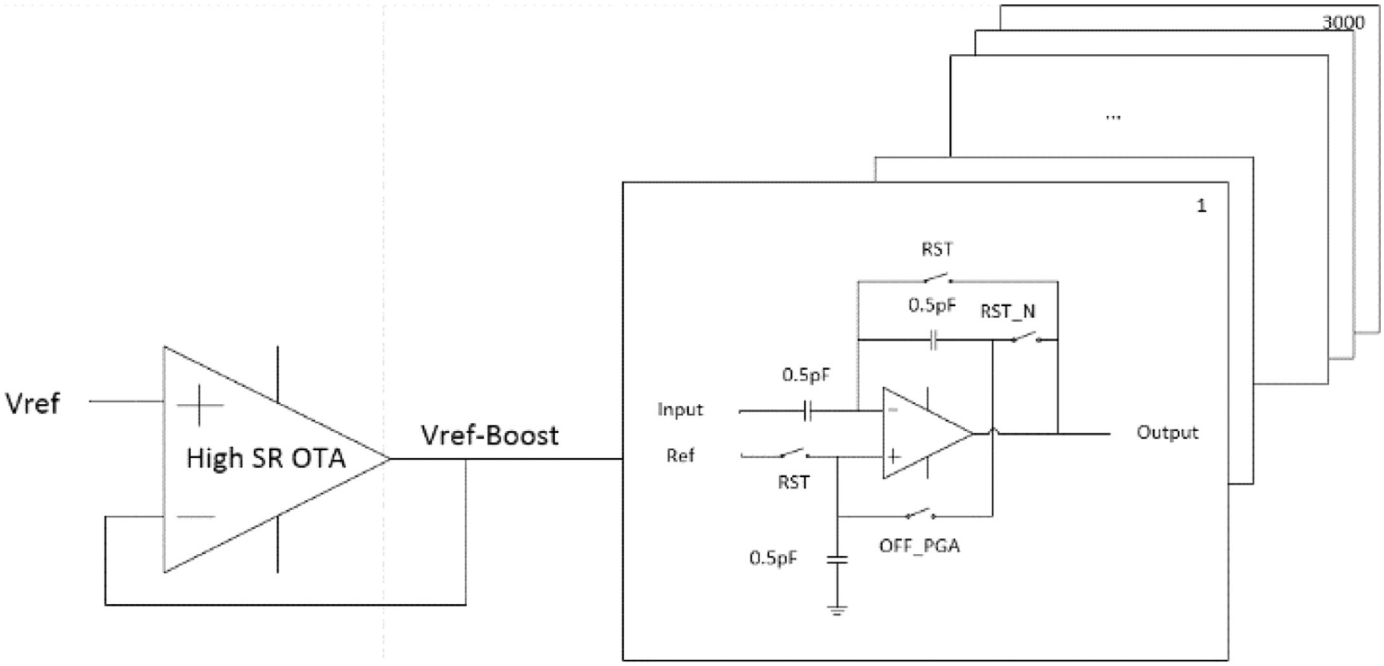

Fig. 22. Simplified view of the 3k PGA reference driver test bench.

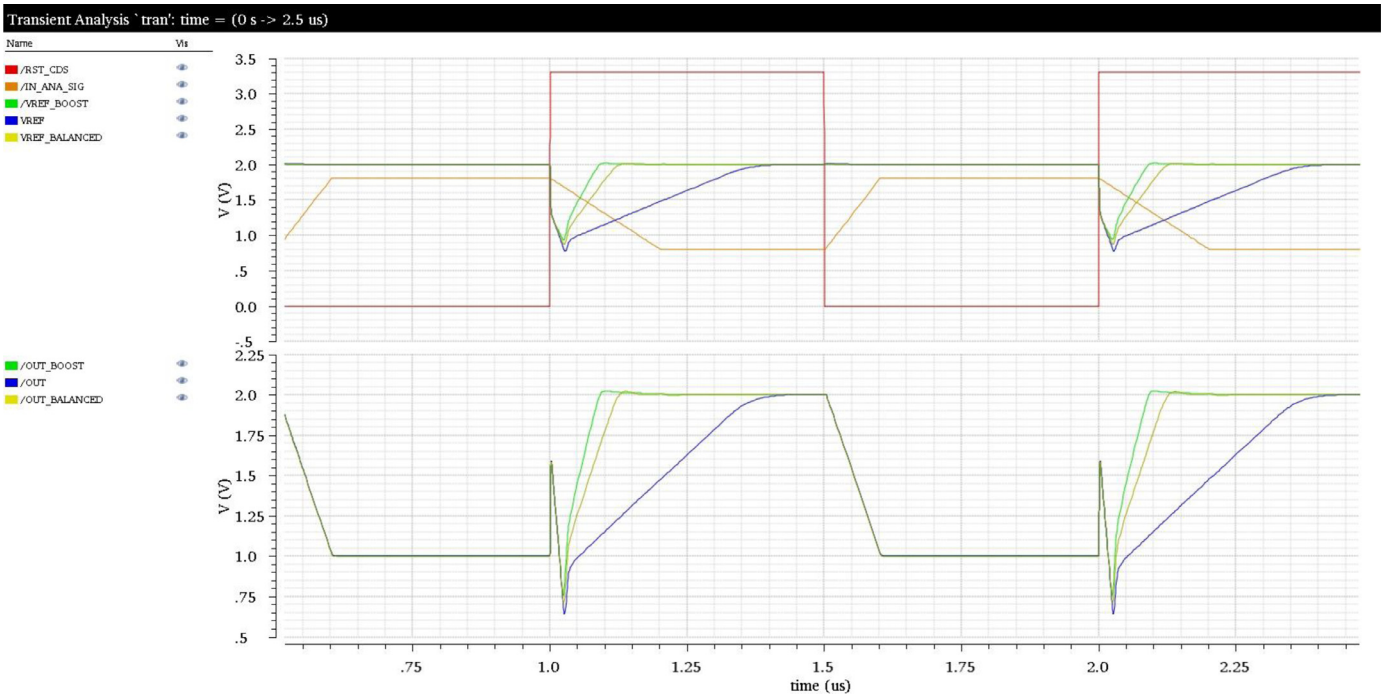

Fig. 23. Transient simulation input and output waves forms, for 3000 PGA reference driver.

Table 3
Current consumption at equal SR.

	For equal output slew-rate of 4 V/us Quiescent current (mA)
Proposed amplifier structure	1.43
Single main amplifier	5.2
Competitor diff. balanced amplifier	1.93

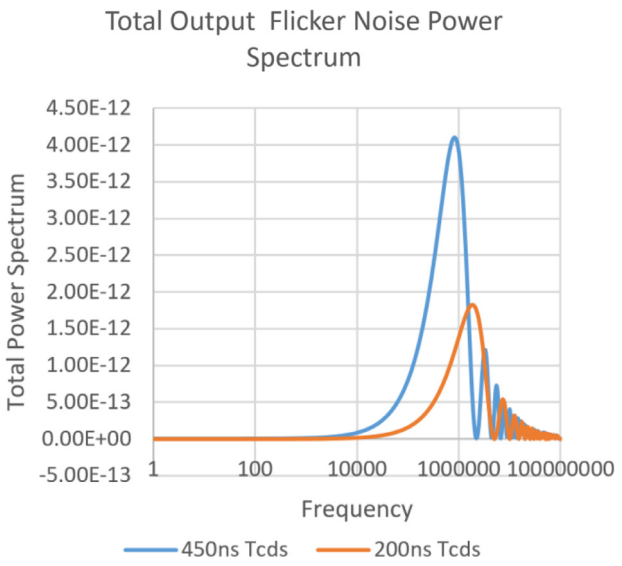

Fig. 24. Flicker noise PSD shaped by 2 different extracted DS transfer functions.

at the PGA output (referred to its reference voltage) by letting the in-pixel amplifier drive the reset value onto the column bus, applying it to the PGA input.

We can notice that the stage's outputs looks similar to the reference voltages, on each driver case. That has to do with the fact that during PGAs reset phase (offset cancelation) their outputs are shorted with their negative differential input, as Figs. 3 and 4 can show. The important part to retain here, is how the references voltages look like.

As can be verified, during PGA reset phase, the offset cancellation takes place and all reference signals were able to recover within the available time (500 ns), given the large signal left from previous light integration. However, the proposed enhanced SR amplifier structure and the best alternative from the literature (the LCMFB) were able to settle faster compared with a regular main rail-to-rail OTA, as we would expect, given the preliminary simulation results. The first one settled in 200 ns while the single rail-to-rail push-pull amplifier has settled around 450 ns. This last one is close to the 500 ns time, which is the time reserved for PGA calibration in the simulation, therefore leaving room for having light signal dependent artifacts such as image lag, if silicon falls in a slow corner process. If this issue occurs, then it would lead to improper behavior of the readout system and generate consecutive non-related signal AD conversions, compromising seriously the CIS image quality.

Finally, Fig. 24 shows the resulting curves from a test flicker PSD multiplied with the power of the readout system DS transfer function, similar to the one on Fig. 6, however in this case for both extracted sampling period cases.

The total area under each curve is the noise variance of the resulting output noise, induced by the considered 1/f noise spectrum test case. The smaller the area, the less is the resulting output flicker RMS noise. And indeed there is a noticeable area reduction from the extracted 200 ns DS time with respect to the 450 ns case, meaning therefore a smaller contribution of the pixel SF flicker noise.

6. Conclusions

In this work, a new output SR enhancement amplifier is proposed and is presented with a simple block level structure. The results shows that the proposal is functional, presents some advantages and it can be made with different types of base amplifiers, providing a generic solution for Very High Slew-Rate Amplifiers.

Considering the results, several conclusions can be withdraw:

- The proposed amplifier structure exhibits 34% higher output SR compared with its competitor LCMFB, for equal quiescent current. However the proposed solution suffers from higher delay, which in turn makes both amplifiers to end up roughly in same settling time. Nevertheless, it is always possible to increase the output devices' size of the boost auxiliary circuit in order to further increase the output SR, without increasing more the DC nominal current of the proposed circuit structure.
- The main amplifier of the proposed circuit can be drawn as a rail-to-rail input amplifier, with the buffer able to drive relatively high and low voltages within the power rails, which does not occurs with its competitor. Moreover, the proposed structure can be also used for high precision applications given that the main OTA is not limited to a specific amplifier architecture, therefore it can be tuned to meet different specifications.
- The proposed structure can be partially implemented, without the need of having both up and down auxiliary branches, depending on the application. For example, if the signal to drive is close to the VDD power rail and if it has mainly to supply current, then the main OTA can be a N-type input differential pair amplifier type with a low side boost auxiliary circuit, saving space, current consumption and still achieve specific and high SR.

From section V results we can point to 3 directions that can be explored in future work: either PGA calibration time is substantially higher than the reference settling time, and by this we make sure no column induced lag will occur, or calibration time is reduced as much as we can so that flicker noise has less effect, or a bit of both previous cases.

Finally, from this work we can conclude that the proposed structure enables faster pixel reset level and signal level sampling frequency, resulting in an improvement in overall flicker noise. Furthermore, it also enables a safe way to avoid column circuitry induced artifacts by means of assuring a complete calibration and offset cancellation of the PGA/DS analogue stage.

Declaration of Competing Interest

None.

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Further reading

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